IN THE SPECIFICATION

Please amend the paragraph beginning on page 37, line 12, as follows:

-- $$+\underline{(u_2 \cdot x^{18} + u_1 \cdot x^{17} + u_0 \cdot x^{16}) \bmod G(x)}_{79} \qquad (\cancel{25}\underline{38})$$

where the underlined computations are carried out in the i-th cycle, for $0 \le i \le 79$. Define the following polynomials:

$$g_0(x) = x^{16} \bmod G(x) \qquad (\cancel{26}\underline{39})$$

$$g_0(x) = \alpha^{120}x^{15} + \alpha^{104}x^{14} + \alpha^{107}x^{13} + \alpha^{109}x^{12} + \alpha^{102}x^{11} + \alpha^{161}x^{10} + \alpha^{76}x^{9} + \alpha^{3}x^{8} + \alpha^{91}x^{7} + \alpha^{191}x^{6} + \alpha^{147}x^{5} + \alpha^{169}x^{4} + \alpha^{182}x^{3} + \alpha^{194}x^{2} + \alpha^{225}x + \alpha^{120}$$

$$g_1(x) = x^{17} \bmod G(x) \qquad (\cancel{27}\underline{40})$$

$$g_1(x) = \alpha^{138}x^{15} + \alpha^{229}x^{14} + \alpha^{18}x^{13} + \alpha^{114}x^{12} + \alpha^{92}x^{11} + \alpha^{28}x^{10} + \alpha^{31}x^{9} + \alpha^{126}x^{8} + \alpha^{233}x^{7} + \alpha^{10}x^{6} + \alpha^{53}x^{5} + \alpha^{240}x^{4} + \alpha^{100}x^{3} + \alpha^{173}x^{2} + \alpha^{156}x + \alpha^{240}$$

$$g_2(x) = x^{18} \bmod G(x) \qquad (\cancel{28}\underline{41})$$

$$g_2(x) = \alpha^{155}x^{15} + \alpha^{32}x^{14} + \alpha^{170}x^{13} + \alpha^{251}x^{12} + \alpha^{106}x^{11} + \alpha^{130}x^{10} + \alpha^{46}x^{9} + \alpha^{160}x^{8} + \alpha^{199}x^{7} + \alpha^{63}x^{6} + \alpha^{16}x^{5} + \alpha^{50}x^{4} + \alpha^{226}x^{3} + \alpha^{251}x^{2} + \alpha^{168}x + \alpha^{3}$$

A block diagram of one three-parallel RS encoder 2200 is shown in FIG. 22. The circuit 2200 of FIG. 22 implements Equation (~~25~~38) by using Equations (~~26~~39), (~~27~~40), and (~~28~~41), and the constant multipliers in these equations are hardwired into an XOR network 2210. In FIG. 22, it can be seen that three input symbols, I_0, I_1, and I_2, are input to the RS encoder 2200. These input symbols, I_0, I_1, and I_2, are multiplied by the appropriate polynomials, $g_0(x)$, $g_1(x)$, and $g_2(x)$, respectively, in the XOR network 2210, and the additions shown by reference numeral 2220 are performed. For example, the content of register_0 is added to the content at location 3 from the XOR network 2210 and the result is placed in register_3. Similarly, the content of register_3 is added to the content at location 6 from the XOR network 2210 and the result is placed in register_6.

As the incoming data to the RS encoder 2200 is assumed to have 239 information symbols followed by 16 zero symbols, i.e., a zero symbol is actually padded at the end of the incoming information sequence instead of the beginning as required by

Equation (~~25~~38), the incoming data needs to be buffered and reformatted to suit Equation (~~25~~38).

The conversion sequence 2300 for performing buffering and reformatting is shown in FIG. 23. Sequence 2300 takes care of the format difference by delaying the processing of the last received symbol to the next cycle. Sequence 2300 works as follows. From the system level, the external inputs 2351 (i.e., u_{238}, u_{237}, and u_{236}) are available during the first cycle (i.e., cycle 0 in FIG. 23). However, the first term of Equation (~~25~~38) is the following: $(0 \cdot x^{18} + u_{238} \cdot x^{17} + u_{237} \cdot x^{16})$. This means that the available symbols 2351 are not the appropriate symbols to meet the requirements of Equation (~~25~~38). Additionally, the next term of Equation (~~25~~38) is $(u_{236} \cdot x^{18} + u_{235} \cdot x^{17} + u_{234} \cdot x^{16})$, which means that u_{236} is needed for the second cycle (i.e., cycle 1 of FIG. 23), but not for the first cycle.

To solve this dilemma, in addition to three-parallel encoder 2200, there is also a delay 2355 that delays u_{236} one cycle. Delay 2355 is part of delay circuit 2370. Additionally, circuit 2370 inputs a zero as the highest order symbol in cycle 0. Thus, in cycle 0, the three-parallel encoder 2200 is used to properly calculate $(0 \cdot x^{18} + u_{238} \cdot x^{17} + u_{237} \cdot x^{16})$. Three-parallel encoder 2200 passes u_{238} and u_{237}, but these are delayed, using delays 2360, so that u_{238}, u_{237}, and u_{236} arrive unchanged out of the encoder 2300 at the same time (as c_{254}, c_{253}, and c_{252}), which occurs during cycle 1. Also during cycle 1, the information symbols u_{235}, u_{234}, and u_{233} are received, u_{233} is delayed, and the $(u_{236} \cdot x^{18} + u_{235} \cdot x^{17} + u_{234} \cdot x^{16})$ calculation is performed. This process continues for 79 cycles, at which time all redundancy symbols have been calculated by the three-parallel encoder 2200. Note that one redundancy symbol, c_{15}, is output during cycle 79. The rest of the redundancy symbols merely have to be read out of three-parallel encoder 2200. This is performed by inputting zero symbols into the encoder 2200 for five cycles and retrieving the other 15 redundancy symbols, c_{14} through c_0. Circuit 2370 is used to input zeros for the appropriate number of cycles. Optionally, a system (not shown) into which three-parallel encoder 2200 is placed can input zeros into circuit 2370.--